

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:  
a plurality of DRAM circuits;  
a control circuit that receives a test control  
5 signal to perform a test control in which said  
plurality of RAM circuits are tested while the access  
to said plurality of DRAM circuits is subsequently  
changed for each row;  
an input selector that is controlled by said  
10 control circuit and inputs a DRAM macro signal to said  
plurality of DRAM circuits at the time of a test; and  
an output selector that is controlled by said  
control circuit, and outputs output signals of said  
plurality of DRAM circuits sequentially to a macro  
15 output terminal at the time of the test.
2. A semiconductor integrated circuit according  
to claim 1, wherein said control circuit is directly  
connected to a control signal input terminal to be  
controlled from said control signal input terminal and  
20 thereby the control circuit is directly controlled from  
said control signal input terminal.
3. A semiconductor integrated circuit according  
to claim 1, wherein said input selector that is  
controlled by said control circuit to input a DRAM  
25 macro signal to one of said plurality of DRAM circuits  
at the time of a normal operation.
4. A semiconductor integrated circuit according

to claim 3, wherein said control circuit is directly  
connected to a control signal input terminal to be  
controlled from said control signal input terminal and  
thereby the control circuit is directly controlled from  
5 said control signal input terminal.

5. A semiconductor integrated circuit according  
to claim 1, wherein said output selector is controlled  
by said control circuit to output an output signal of  
one of said plurality of DRAM circuits to the macro  
10 output terminal at the time of a normal operation.

6. A semiconductor integrated circuit according  
to claim 5, wherein said control circuit is directly  
connected to said control signal input terminal to be  
directly controlled from said control signal input  
15 terminal and thereby is controlled directly from said  
control signal input terminal.

7. A semiconductor integrated circuit according  
to claim 1, wherein said control circuit performs a  
test control of said plurality of DRAM circuits in such  
20 a manner that the access to first rows of said  
plurality of DRAM circuits is performed while  
successively changing the access to said plurality of  
DRAM circuits, and, following the access to the first  
rows of said plurality of DRAM circuits, the same  
25 access as that to the first rows of said plurality of  
DRAM circuits is performed from the next rows to the  
last rows of said plurality of DRAM circuits while

successively changing the access to said plurality of  
DRAM circuits for each row.

8. A semiconductor integrated circuit according  
to claim 7, wherein said control circuit is connected  
5 directly to said control signal input terminal to be  
directly controlled from the control signal input  
terminal and thereby the control circuit is directly  
controlled from said control signal input terminal.

9. A semiconductor integrated circuit comprising:  
10 a plurality of DRAM circuits;

a plurality of control circuits each of which is  
provided corresponding to one of said plurality of DRAM  
circuits, and receives a test control signal to perform  
a test control of said corresponding one DRAM circuit;  
15 and

an output selector that is controlled by said  
control signal, and outputs output signals of said  
plurality of DRAM circuits sequentially to a macro  
output terminal at the time of a test.

10. A semiconductor integrated circuit according  
to claim 9, wherein said control circuits are directly  
connected to a control signal input terminal to be  
controlled from said control signal input terminal and  
thereby the control circuits are directly controlled  
25 from said control signal input terminal.

11. A semiconductor integrated circuit according  
to claim 9, further comprising an input selector for

receiving a DRAM macro signal.

12. A semiconductor integrated circuit according to claim 11, wherein said control circuits are directly connected to a control signal input terminal to be  
5 controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

13. A semiconductor integrated circuit according to claim 9, wherein said output selector is controlled  
10 by said control circuit to output an output signal of one of said plurality of DRAM circuits to the macro output terminal at the time of a normal operation.

14. A semiconductor integrated circuit according to claim 13, wherein said control circuits are directly  
15 connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

15. A semiconductor integrated circuit according to claim 9, wherein said control circuits performs a  
20 test control of said plurality of DRAM circuits in such a manner that the access to first rows of said plurality of DRAM circuits is performed while successively changing the access to said plurality of  
25 DRAM circuits, and, following the access to the first rows of said plurality of DRAM circuits, the same access as that to the first rows of said plurality of

DRAM circuits is performed from the next rows to the last rows of said plurality of DRAM circuits while successively changing the access to said plurality of DRAM circuits for each row.

5           16. A semiconductor integrated circuit according to claim 15, wherein said control circuits are directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled  
10           from said control signal input terminal.

          17. A semiconductor circuit comprises:  
          a plurality of DRAM circuits;  
          a control circuit that receives a control signal and controls said plurality of DRAM circuits  
15           simultaneously and independently from each other;  
          an input selector for supplying a DRAM macro signal input to one of said plurality of DRAM circuits;  
          an output selector that selects an output signal of one of said plurality of DRAM circuits and outputs  
20           the output signal to a macro output terminal.

          18. A semiconductor integrated circuit according to claim 17, wherein on receiving the control signal, said control circuit controls said plurality of DRAM circuits so that data is read from said plurality of  
25           DRAM circuits sequentially and transferred to the outside of the DRAM circuits.

          19. A semiconductor integrated circuit according

to claim 18, wherein said control circuit supplies the bank active signal BACT to one of said plurality of DRAM circuits and then controls said output selector in a manner such that said output selector selects the output signal of said one DRAM circuit, and then, after the data is read and outputted from columns of said one DRAM circuit sequentially, supplies a bit line precharge signal BPRC to said one DRAM circuit, and

said control circuit supplies the bank active signal BACT to another DRAM circuit while supplying a read signal READ to said one DRAM circuit, and controls said output selector so as to select the output signal of said another DRAM circuit while supplying the bit line precharge signal BPRC to said one DRAM circuit.